ABSTRACT OF THE DISCLOSURE

In one set of embodiments the invention comprises a highly accurate, low-power, compact size DAC utilizing charge redistribution techniques. Two complementary conversions may be performed and added together to form a final DAC output voltage by performing charge redistribution a first time, and again a second time in a complementary fashion, followed by a summing of the two charge distributions, in effect canceling the odd order capacitor mismatch errors. By canceling all odd order mismatch errors the accuracy of the DAC may become a function of the square of the mismatch of the two capacitors, resulting in greatly increased accuracy. When performing the complementary conversions for multiple bits, the sequence in which each of the two capacitors is charged may be determined to minimize the even-order errors, especially second-order errors. The DEM technique may be applied, in conjunction with the complementary conversions, with less oversampling than required by current DEM implementations, resulting in even-order errors being substantially reduced in addition to all odd-order errors being eliminated.